ECE 482

Fall 2026

Review Notes for ECE 482 (Digital IC Design)

These notes aren't fully comprehensive.

Aniketh Tarikonda (aniketh8@illinois.edu)

Contents

1 Intro & MOSFET Static Analysis

- By the textbook convention, we have a positive drain current when it flows into the drain.
  - NMOS drain current should be positive, PMOS should be negative.
- Industry is going towards SiP instead of SoC because of yield issues and reticle sizes making large monolithic dies unlikely

Technology Scaling

- generation is $18 - 24$ months
- feature sizes shrink $\sim 0.7x$ per generation, $2x$ transistors per area (insert Dennard Scaling mention here)
- STI (the other one) stands for shallow trench isolation and can prevent leakage between adjacent transistors
- Moore's Law

Supply Voltage Scaling

- if V_{DD}, L_{gate}, T_{ox} reduce by an identical factor, the lateral and vertical electric fields stay the same, so performance also stays the same.
- power is reduced as well
- historically, L_{gate} was shrunk more aggressively than supply voltage, so transistor feature size scaling virtually stopped at 90nm

Noise

- one of the quality metrics of a digital IC
- can impact the robustness/functionality of a digital IC
  - inductive coupling
  - capacitative coupling
  - power and ground noise
- **VTC** - Voltage-Transfer Characteristics
  - plot of output voltage as a function of input voltage

Important Parts of a VTC Curve (For an Inverter)

- V_{OL} - output low
- V_{OH} - output high
- V_{IL} - input low (point where derivative of VTC is -1 for the first time)
- V_{IH} - input high (point where derivative of VTC is -1 for the second time)
- V_M - inverter switching threshold (point where $V_{\text{out}}(V_{\text{in}}) = V_{\text{in}}$)
- V_{OL} and V_{OH} are defined wrt. each other.

- In the case of the inverter, we can create a flip-flop by hooking the inputs/outputs of two inverters together.
  - there are two stable operating points ($(V_{\text{OH}}, V_{\text{OL}})$ and $(V_{\text{OL}}, V_{\text{OH}})$), and a metastable point

Delay

- t_p - propagation delay from when $V_{\text{in}} = V_{50}$ until $V_{\text{out}} = V_{50}$
  - $V_{50} = \frac{V_{\text{OH}} + V_{\text{OL}}}{2}$
- $\boldsymbol{t_{\text{pLH}} \neq t_{\text{pHL}}}$ necessarily
- One of the ways we can measure delay is through a **ring oscillator**
  - odd number of inverters connected in a circular chain
  - period T of the oscillation is given by $T = 2t_pN$ where N is the number of inverters

Long-Channel Model

When $V_{\text{gs,n}} < V_{\text{T, n}}$ or $V_{\text{gs,p}} > V_{\text{T, p}}$, $I_{\text{ds}} = 0$

When $V_{\text{ds,n}} < V_{\text{dsat,N}}$ or $V_{\text{ds,p}} > V_{\text{dsat,p}}$, $I_{\text{ds}} = \mu C_{\text{ox}}\left(\frac{W}{L}\right)\left(V_{\text{ov}}V_{\text{ds}} - \frac{1}{2}V_{\text{ds}}^2\right)$

When $V_{\text{ds,n}} \geq V_{\text{dsat,N}}$ or $V_{\text{ds,p}} \leq V_{\text{dsat,p}}$, $I_{\text{ds}} = \frac{1}{2}\mu C_{\text{ox}}\left(\frac{W}{L}\right)\left(V_{\text{ov}}^2\right)$

Instead of using μC_{ox}, we use k'
- under our convention, PMOS k' should be negative

Threshold Voltage

$V_t = V_{\text{t0}} + \gamma\left(\left|\sqrt{V_{\text{sb}} - 2\varphi_F}\right| - \sqrt{|-2\varphi_F|}\right)$
- By design $V_{\text{sb}} \geq 0$ for NMOS and $V_{\text{sb}} \leq 0$ for PMOS

Short vs. Long Channel
- short channel enters saturation "earlier" at a lower V_{ds}
- in the saturation region, the slope of the short channel device is higher
- no apparent quadratic relation with V_{gs} in saturation region.

Velocity Saturation
- carrier velocity increases linearly with E-field only up to a few kV/cm
- there are a few equations for this, the basic idea being that we define two regions where $E_{\text{lat}} < E_c$, and then $E_{\text{lat}} = E_c$ where E_c is the critical E-field.

Non-Ideal Effects
- channel-length modulation & DIBL, to account for these, we add V_{ds} related terms to the IV equation.
- $u_{\text{eff}} = f\left(V_{\text{gs}}\right)$, in other words, $T_{\text{ox, eff}} \neq T_{\text{ox, physical}}$

To account for these short-comings of the Long-Channel Model, we introduce the **Short-Channel Model**.

- $I_{\text{ds}} = k\big((V_{\text{gs}} - V_t)V_{\text{min}} - \frac{1}{2}V_{\text{min}}^2\big)(1 + \lambda V_{\text{ds}})$
- $V_{\text{min,n}} = \min\big(V_{\text{ds}}, V_{\text{gt}}, V_{\text{dsat,n}}\big)$ or $V_{\text{min,p}} = -\min\big(|V_{\text{ds}}|, |V_{\text{gt}}|, |V_{\text{dsat,p}}|\big)$
- high V_t transistor is often called "low power" because leakage current is very low.
- low V_t transistor is often called "high performance" because ON state current will be higher.

Subthresold Operation

- exponential dependence of I_{ds} on V_{gs} in the subthreshold region.
- neither long or short channels accurately represent I_{ds} in the subthreshold region.
- subthreshold V_t is defined as the V_{gs} at which point $I_{\text{d}} = 100\ [\text{nA}] * \big(\frac{W}{L}\big)$
  - IV plot is linear below this point, assuming you're using a semi-log plot.
  - $I_{\text{d, threshold}} = 100\big(\frac{W}{L}\big)10^{\frac{V_{\text{gs}} - V_{\text{t}}}{S}}\ [\text{nA}]$
- **there is a parasitic BJT within a MOSFET**, which is where the exponential relation with V_{gs} comes from.

2 Dynamic Analysis of CMOS Inverter

- If we have a square wave input, on the rising edge of the input:
  - our $V_{\text{ds, n}} = V_{\text{dd}}$
- After t_{pHL}, $V_{\text{ds}} = \frac{V_{\text{dd}}}{2}$
- Doing KCL on the output node, we get the following equation

$$C_L \frac{dV_{\text{out}}}{dt} = k_{n'} \left(\frac{W}{L}\right) \left[(V_{\text{dd}} - V_{\text{tn0}})V_{\text{dsatn}} - \frac{1}{2}V_{\text{dsatn}}^2\right](1 + \lambda_n V_{\text{out}})$$

$$\int_{V_{\text{dd}}}^{\frac{V_{\text{dd}}}{2}} \frac{C_L}{I_{\text{dn}}} \, \mathrm{d}V_{\text{out}} = \int_0^{t_{\text{pHL}}} \mathrm{d}t = t_{\text{pHL}}$$

$$\text{assuming } (1 + \lambda_n V_{\text{out}}) \approx 1 \tag{1}$$

$$I_{\text{dn}} \approx \left(\frac{W}{L}\right) k_{n'}(\ldots) = \left(\frac{W}{L}\right) I_{\text{dsat,n}}$$

$$t_{\text{pHL}} = \frac{LC_L}{WI_{\text{satn}}} \int_{V_{\text{dd}}}^{\frac{V_{\text{dd}}}{2}} \mathrm{d}V_{\text{out}} = \frac{LC_L V_{\text{dd}}}{2WI_{\text{satn}}}$$

Ultimately, we have a similar process when calculating t_{pLH} –the NMOS is in cutoff and the PMOS is in triode/saturation. Thus, we end up with

$$t_{\text{pLH}} = \frac{LC_L V_{\text{dd}}}{2WI_{\text{satp}}} \tag{2}$$

Using an RC model of delay, we end up with

$$\begin{aligned} t_{\text{pHL}} &= \frac{0.69}{S} R_{\text{n0}} C_L \\ t_{\text{pLH}} &= \frac{0.69}{S\beta} R_{\text{p0}} C_L \end{aligned} \tag{3}$$

where $S = \frac{W_{\text{N}}}{W_{\text{min}}}$ and $\beta = \frac{W_{\text{P}}}{W_{\text{N}}}$

2.1 MOS Capacitances

- C_{drain} is the intrinsic (self-loading) capacitance of the MOSFET
- C_{gate} is the fanout/extrinsic capacitance
- C_{wire} is the (somewhat negligible) wire capacitance
- **5 capacitor model**

- $C_{\text{gb}}, C_{\text{gd}}, C_{\text{gs}}, C_{\text{sb}}, C_{\text{db}}$
- we don't really care about C_{sb}

Because of Miller's theorem, we can view C_{gd} as two separate capacitors (one on input, one on output)

Theres also overlap capacitance (overlap between gate and drain/source)
- added capacitance form **fringing fields**

Operation Region	C_{gb}	C_{gs}	C_{gd}
Cut-off	$C_{\text{ox}}WL$	C_oW	C_oW
Triode	0	$\frac{C_{\text{ox}}WL}{2} + C_oW$	$\frac{C_{\text{ox}}WL}{2} + C_oW$
Saturation	0	$\frac{2C_{\text{ox}}WL}{3} + C_oW$	C_oW

2.1.1 PN-junction Capacitances
- textbook assumes LOCOS (local oxidation of silicon), which is old, and kind of obsolete for post $250\mu m$ processes.
- $C_{\text{diff}} = C_{\text{bottom}} + C_{\text{sidewall}} = C_J * \text{Area} + C_{\text{JSW}} * \text{Perimeter} = C_J L_S W + C_{\text{JSW}} * (2L_S + W)$
- $C_J = \frac{C_{\text{J0}}}{\left(1+\frac{V_J}{\varphi_B}\right)^m}$ where V_J is the voltage drop across the PN junction, $V_J \leq 0$ for drain-body and source-body connection.

Non-Linear Capacitances
- often times, we will need to use average capacitances.
- $\overline{C} = \frac{1}{V_j - V_i}\int_{V_i}^{V_j} C(V)\,\mathrm{d}V$ where $C(V) = \frac{C_{\text{J0}}}{\left(1+\frac{V}{\varphi_B}\right)^m}$
- we end up with $\overline{C} = K_{\text{eq}} C_{\text{j0}}$